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IET CNF	IET Conference Proceeding
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1 From Electron Mobility to Logical Structure: A View of Integrated Circuits
Wesley A. Clark
September 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 3
Publisher: ACM Press
Full text available: pdf(3.29 MB) Additional Information: full citation, references, citings, index terms

2 Silicon trends and limits for advanced microprocessors
Mark Bohr
March 1998 **Communications of the ACM**, Volume 41 Issue 3
Publisher: ACM Press
Full text available: pdf(221.08 KB) Additional Information: full citation, references, citings, index terms

3 Nanowire-based programmable architectures
André Dehon
July 2005 **ACM Journal on Emerging Technologies in Computing Systems (JETC)**, Volume 1 Issue 2
Publisher: ACM Press
Full text available: pdf(2.25 MB) Additional Information: full citation, abstract, references, citings, index terms

Chemists can now construct wires which are just a few atoms in diameter; these wires can be selectively field-effect gated, and wire crossings can act as diodes with programmable resistance. These new capabilities present both opportunities and challenges for constructing nanoscale computing systems. The tiny feature sizes offer a path to economically scale down to atomic dimensions. However, the associated bottom-up synthesis techniques only produce highly regular structures and come with high ...

Keywords: Defect tolerance, Manhattan mesh, nanowires, programmable interconnect, programmable logic arrays, stochastic construction, sublithographic architecture

4 Topological analysis for VLSI circuits
Paul Losleben, Kathryn Thompson

June 1979 **Proceedings of the 16th Conference on Design automation DAC '79**
Publisher: IEEE Press
Full text available: pdf(827.63 KB) Additional Information: full citation, abstract, citings, index terms

Algorithms are presented which use a bit map approach to derive connectivity checks, design rule checks, and electrical parameters for VLSI circuit artwork.

5 A set of programs for MOS design
G. Sakauye, A. Lubiw, J. Royle, R. Epplett, J. Twidale, E. Shew, E. Attfield, F. Brglez, P. Wilcox
June 1981 **Proceedings of the 18th conference on Design automation DAC '81**
Publisher: IEEE Press
Full text available: pdf(778.19 KB) Additional Information: full citation, abstract, references, citings, index terms

A set of programs used in the design of custom hand packed and standard cell MOS circuits is described. The programs cover logic simulation, filter analysis, circuit simulation, timing simulation, circuit extraction from layout, design tolerance checking, connectivity checking and user interface facilities. A cell documentation system is used to tie together the various design support packages.

6 An integrated mask artwork analysis system
Takashi Mitsuhashi, Toshiaki Chiba, Makoto Takashima, Kenji Yoshida
June 1980 **Proceedings of the 17th conference on Design automation DAC '80**
Publisher: ACM Press
Full text available: pdf(712.44 KB) Additional Information: full citation, abstract, references, citings, index terms

A new LSI artwork analysis and processing system, called EMAP, is described with algorithms, a database schema and applications. EMAP provides the designer with the artwork verification and processing tools which include mask artwork processing, geometrical design rule checking, connectivity analysis and electrical circuit parameter calculation. The circuit connectivity data derived from the mask artwork data is used for input to a logic simulator, a timing simulator, a circuit simulator an ...

7 Automatic circuit analysis based on mask information
B. T. Preas, B. W. Lindsay, C. W. Gwyn
June 1976 **Proceedings of the 13th conference on Design automation DAC '76**
Publisher: ACM Press
Full text available: pdf(769.12 KB) Additional Information: full citation, abstract, references, citings, index terms

A Circuit MAsk Translator (CMAT) code has been developed which converts integrated circuit mask information into a circuit schematic. Logical operations, pattern recognition, and special functions are used to identify and interconnect diodes, transistors, capacitors, and resistances. The circuit topology provided by the translator is compatible with the input required for a circuit analysis program.

8 A case study in process independence
Natalie Royal, John Hunter, Irene Buchanan
June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation DAC '85**
Publisher: ACM Press
Full text available: pdf(630.58 KB) Additional Information: full citation, abstract, references, index terms

By taking input from both a design description file and a file which contains the design rules of the target process, a silicon compiler software system can produce full artwork

layouts for a variety of different processes. A specific example is used here to illustrate the complexities of incorporating the option of process independence in a system aimed at single metal interconnect CMOS.

9 Philo-a VLSI design system

R. Donze, J. Sanders, M. Jenkins, G. Sporzynski

January 1982 **Proceedings of the 19th conference on Design automation DAC '82**

Publisher: IEEE Press

Full text available: pdf(594.87 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a design system capable of designing chips in the range of 5K to 7K equivalent three-way NOR gates. A key feature of the system is the ability to design chips with large macros (RAMs and PLAs). This design system is part of IBM's corporate-wide Engineering Design System (EDS). EDS provides the capabilities of logic simulation, automatic placement and wiring, checking, and test pattern generation (I). This paper describes the key capabilities of the system, specifically ...

10 Deep Sub-Micron IDDQ Testing: Issues and Solutions

M. Sachdev

March 1997 **Proceedings of the 1997 European conference on Design and Test EDTC '97**

Publisher: IEEE Computer Society

Full text available: pdf(1.03 MB) Additional Information: full citation, abstract, citings Publisher Site

The effectiveness of I/sub DDQ/ testing in deep sub-micron is threatened by the increased transistor sub-threshold leakage current. In this article, we survey possible solutions and propose a deep sub-micron I/sub DDQ/ test mode. The methodology provides means for unambiguous measurements of I/sub DDQ/ components and defect diagnosis. The effectiveness of the test mode is demonstrated with a real life example.

Keywords: CMOS integrated circuits, deep submicron IDDQ testing, transistor sub-threshold leakage current, defect diagnosis, CMOS IC

11 Layout tools for analog ICs and mixed-signal SoCs: a survey

Rob A. Rutenbar, John M. Cohn

May 2000 **Proceedings of the 2000 international symposium on Physical design ISPD '00**

Publisher: ACM Press

Full text available: pdf(247.03 KB) Additional Information: full citation, references

12 MAP: A user-controlled automated Mask Analysis Program

Cheryl L. Mitchell, John M. Gould

January 1974 **Proceedings of the 11th workshop on Design automation DAC '74**

Publisher: IEEE Press

Full text available: pdf(629.51 KB) Additional Information: full citation, abstract, citings, index terms

The Mask Analysis Program is a totally general and application independent FORTRAN program for the analysis and manipulation of graphic data. It is particularly useful in integrated circuit design analysis.

13 The automatic recognition of silicon gate transistor geometries: An LSI design aid

program
Ivan Dobes, Ron Byrd
June 1976 **Proceedings of the 13th conference on Design automation DAC '76**
Publisher: ACM Press

Full text available: pdf(592.57 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a computer program (SIGAP) that analyzes digitized LSI mask data for valid and invalid Silicon Gate transistor geometries. The program's function, as well as the topological mapping technique used, are described. The SIGAP techniques can be adopted to a variety of artwork data preparation tasks, such as elimination of redundancy, overlap creation, area shrink/expand, the decomposition of polygons to equivalent rectangles or vice versa and performing Boolean operations b ...

14 Spin MOSFETs as a basis for spintronics
Satoshi Sugahara, Masaaki Tanaka
May 2006 **ACM Transactions on Storage (TOS)**, Volume 2 Issue 2
Publisher: ACM Press
Full text available: pdf(427.11 KB) Additional Information: full citation, abstract, references, index terms

This article reviews a recently proposed new class of spin transistors referred to as spin metal-oxide-semiconductor field-effect transistors (spin MOSFETs), and their integrated circuit applications. The fundamental device structures, operating principle, and theoretically predicted device performance are presented. Spin MOSFETs potentially exhibit significant magnetotransport effects, such as large magneto-current, and also satisfy important requirements for integrated circuit applications suc ...

Keywords: MOSFETs, Spintronics, spin MOSFETs, spin transistors

15 Analog design and modeling: T-shaped association of transistors: modeling of multiple channel lengths and regular associations
Alessandro Girardi, Fernando P. Cortes, Eduardo Conrad, Sergio Bampi
September 2005 **Proceedings of the 18th annual symposium on Integrated circuits and system design SBCCI '05**
Publisher: ACM Press
Full text available: pdf(795.32 KB) Additional Information: full citation, abstract, references, index terms

This work presents an analysis of a new type of composite transistor specially suited for the design of analog integrated circuits: the T-shape association of transistors. This association is composed by non-equal size unit transistors arranged in a series-parallel array with common gate, which can substitute the conventional rectangular transistors with advantages in some aspects, such as better high-frequency performance, lower output conductance and layout regularity. Dedicated tools that aut ...

Keywords: MOSFET, analog design, associations of transistors, modeling

16 Aesop: a tool for automated transistor sizing
K. S. Hedlund
October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation DAC '87**
Publisher: ACM Press
Full text available: pdf(794.96 KB) Additional Information: full citation, abstract, references, citings, index terms

This work addresses the problem of automating the electrical optimization of combinatorial

MOS circuits. Improvements to a circuit's speed, area and power consumption are sought through modifications to the transistor sizes in the circuit; no changes in the circuit structure, number of gates or clocking are introduced. Linear algorithms are presented for computing optimal transistor sizes to minimize delay, area or power. These algorithms are implemented in an interactive tool, Aesop. Aesop ...

17 Design rule checking and analysis of IC mask designs

B. W. Lindsay, B. T. Preas

June 1976 **Proceedings of the 13th conference on Design automation DAC '76**

Publisher: ACM Press

Full text available: pdf(619.91 KB) Additional Information: full citation, abstract, references, citings, index terms

An efficient method of producing logical combinations of integrated circuit (IC) masks in numerical form leads to a generalized design rule checking program. The union (OR), intersection (AND) and the complements, as well as topological classification and simple geometric operations, are provided through a set of LOGical MASk Checking (LOGMASC) commands, allowing the designer to construct, for the given IC technology, a tailored set of design rule checks. These range from simple tolerance c ...

18 Hybrid CMOS/nanoelectronic digital circuits: devices, architectures, and design automation

A. DeHon, K. K. Likharev

May 2005 **Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design ICCAD '05**

Publisher: IEEE Computer Society

Full text available: pdf(352.84 KB) Additional Information: full citation, abstract

Physics offers several active devices with nanometer-scale footprint, that can be best used in combination with a CMOS subsystem. Such hybrid circuits offer the potential for high defect tolerance combined with unparalleled performance. In this tutorial, we highlight key issues and architectural alternatives for this promising technology and outline the challenges posed by the hybrid circuits pose for design automation.

19 Transistor Flaring in Deep Submicron-Design Considerations

Vipul Singhal, C. B. Keshav, K. G. Surnanth, P. .. R. Suresh

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design ASP-DAC '02**

Publisher: IEEE Computer Society

Full text available: pdf(1.00 MB) Additional Information: full citation

Publisher Site

Keywords: Design for Manufacturability (DFM), Deep Submicron (DSM), pullback, photolithography, Subwavelength-lithography, Optical Proximity Correction (OPC), SPICE-models, standard-ce1l library.

20 Double-gate SOI devices for low-power and high-performance applications

K. Roy, H. Mahmoodi, S. Mukhopadhyay, H. Ananthan, A. Bansal, T. Cakici

May 2005 **Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design ICCAD '05**

Publisher: IEEE Computer Society

Full text available: pdf(783.31 KB) Additional Information: full citation, abstract

Double-gate (DG) transistors have emerged as promising devices for nano-scale circuits

due to their better scalability compared to bulk CMOS. Among the various types of DG devices, quasi-planar SOI FinFETs are easier to manufacture compared to planar double-gate devices. DG devices with independent gates (separate contacts to back and front gates) have recently been developed. DG devices with symmetric and asymmetric gates have also been demonstrated. Such device options have direct implications ...

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